

Revisiting the Path to Burn-in

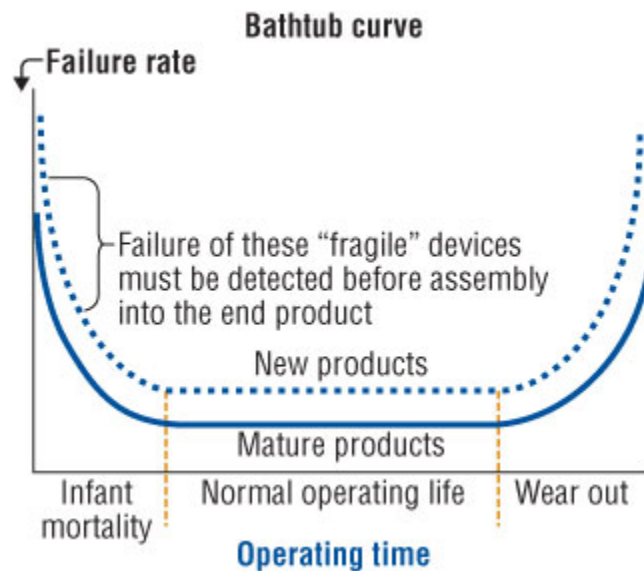
by James A. Forster, Ph.D., Antares Advanced Test Technologies

As IC manufacturers rely more on the burn-in process to bring many of the latest devices from leading-edge fabs to consumers, it is important to truly understand burn-in test. As feature size is reduced into the nanometer range, designers can place more circuits on a square of silicon. As the number of transistors and the total amount of circuitry on a chip increases, the potential for a defect increases, leading to immediate or future failures. Because of the complexity of the processes used during manufacturing, some chips may pass initial QC test but fail after a short time. These devices must be identified and scrapped before assembly. Burn-in lets the manufacturer identify these tentative devices and remove them from the population.

Military Standard 883G describes burn-in as "for the purpose of screening or eliminating marginal devices, those with inherent defects or defects resulting from manufacturing aberrations that cause time and stress dependent failures. In the absence of burn-in, these defective devices would experience infant mortality or early lifetime failures under use conditions. Therefore, it is the intent of this screen to stress microcircuits at or above maximum rated operating conditions or to apply equivalent screening conditions, which will reveal time- and stress-dependent failure modes with equal or greater sensitivity."

Typically, many devices produced in leading-edge fabs — DDR memory, microprocessors — require burn-in to ensure reliability. Flash memory and many DSPs might only be burned-in during the qualification process to demonstrate and validate the process yield. Once the semiconductor processing technology is proven and device reliability meets specific requirements, burn-in can be eliminated.

The three phases in device failure rates over a period of time are illustrated in a typical reliability curve-of-failure rate vs. time (Figure 1). Fragile devices will fail soon after manufacture (infant mortality) as shown by the high initial failure rate. The failure rate is then flat as other types of "random" failures occur. After some time, when the product comes to the end of its useful life, the failure rate will increase. Manufacturing and reliability engineers must identify and remove fragile devices so that end-product reliability is not compromised.



The process to identify or cull these fragile devices is burn-in. This involves stressing the part to force potential failure. The devices are stressed thermally and electrically — placed in an oven at up to 150°C and exposed to voltages as high as 1.5x normal operating voltage. Time spent at temperature can be a few hours to more than 48 hours. Some space applications require two burn-in cycles with total time at temperature of more than 240 hours. Stressing the electrical paths within the chip and thermal expansion issues associated with heating the chip have proven to be the most effective way to force early-

life failures.

The markets that serve burn-in operations include oven manufacturers, board makers, socket suppliers, and makers of auto loader, unload equipment. Challenges for these suppliers include smaller package pitches; higher operating currents; higher temperatures found in automotive applications; and higher test frequencies. No doubt, we can expect semiconductor companies to work to improve their process development to get out of burn-in faster.

James A. Forster, Ph.D., CTO, Antares, has held a variety of management positions dealing with product research and development. Prior to joining Antares he had over 20 years at Texas Instruments' Sensors and Controls Group. He has authored more than 25 technical publications and holds 18 U.S. patents. Dr. Forster earned his B.Sc. (Hons) in mechanical engineering at UMIST, The University of Manchester Institute of Science and Technology. He earned his masters and doctorate at McMaster University in Hamilton, Ontario, Canada. He may be contacted at Antares Advanced Test Technologies, Gilbert, Ariz., ph. (480) 682-6170; james.forster@antares-att.com.

Find this article at:

http://ap.pennnet.com/display_article/354969/36/ARTCL/none/INDUS/1/Revisiting-the-Path-to-Burn-in

Check the box to include the list of links referenced in the article.

Copyright © PennWell Corporation.

